IN THE SPECIFICATION:

Please replace paragraph [0024] at page 7 as follows:

FIG. 4 illustrates a ripple refresh DRAM memory system 400 in accordance with one example of the present disclosure. In this example, the memory system 400 includes a refresh memory block 402 (Block 0) and 7 other memory blocks 404 (Blocks 1 to 7). It is, however, understood by those skilled in the art that the number of blocks within the memory system is scalable and may be changed without deviation to the intention of this disclosure. The refresh memory block 402 actually is also structurally similar to other memory blocks except that it is the first one to be refreshed. Refresh memory block 402 includes a refresh timer 406 and a refresh control circuit 408 that generate the refresh request signals RFRQ[0] and RFRQ[1], respectively, thereby initiating the refresh sequence for the memory system 400 by starting to refresh the first memory block and making the next memory block (Block 1) ready for refresh. After RFRQ[0] is generated for itself, which triggers the refresh process for the refresh memory block, request signals RFRQ[1] is generated for Block 1. Similarly, RFRQ[0] is not generated until Block 7 is refreshed. A Block N of memory blocks 404 includes a refresh control circuit 408 that generates the refresh request signal RFRQ[N+1] for the next memory block, where N+1 is the next memory block. For example, ~~the~~ refresh control circuit 408 of Block 1 generates a refresh signal RFRQ[2], which is fed into Block 2.